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SPARC's STILL GOING STRONG

Fujitsu's New Products Increase Cores, Threads; Sun's Niagara Near

By Kevin Krewell {11/14/05-02}

We've been getting yearly updates from Fujitsu on its SPARC64 server processors for the past four Fall Processor Forums/Microprocessor Forums. Each year, the company extends the roadmap and reviews its steady, if underpublicized, progress in SPARC processor integration

and process migrations. At Fall Processor Forum 2005, Mr. Takumi Maruyama, manager of Fujitsu Limited's Processor Development Department 1 in the Enterprise Server Development Division, returned (he last presented in 2003) to give the latest roadmap update, extending the company's SPARC roadmap out to 2008.

The present Fujitsu product is the 90nm SPARC64 V+, which runs at 2.16GHz. The next processor, finalizing development, is the SPARC64 VI, which is a dual-core processor. While Fujitsu had shown early details of the SPARC64 VI at Fall Processor Forum 2004 (see *MPR*

10/25/04-02, "SPARC Turns 90nm"), Mr. Maruyama provided a progress report and revealed more details of the implementation. Fujitsu is still planning to deliver the chip in 2006; that situation hasn't changed from last year's presentation. The frequency goal for the SPARC64 VI is also still 2.4GHz. The SPARC64 VI+ appears to have slipped slightly, from late 2007 (as positioned in Fujitsu's 2004 presentation) to early 2008 in this updated roadmap. (See Figure 1.)

The power requirements for the dual-core processor are considerably higher than for the single-core SPARC64 V, jumping to 120W from 65W. This isn't an outrageous

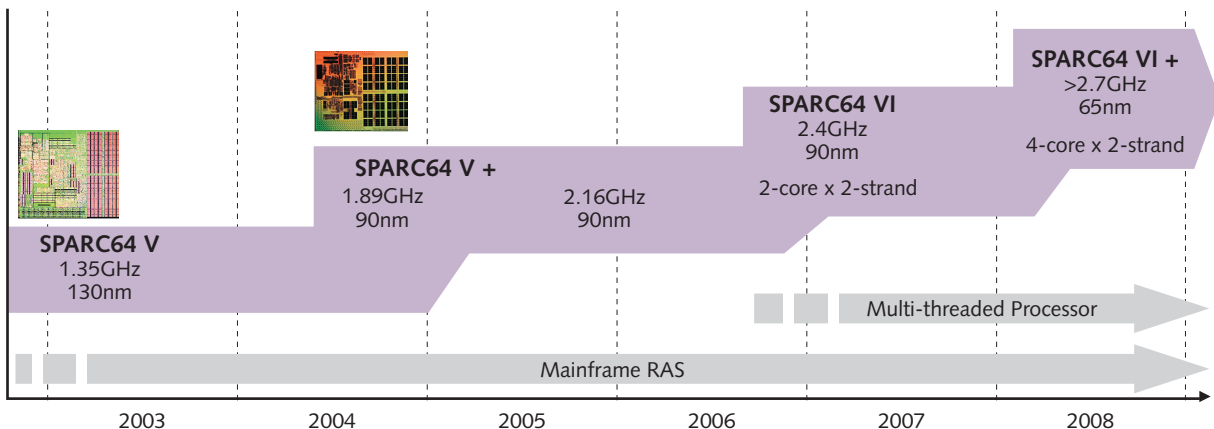


Figure 1. Fujitsu's latest SPARC64 roadmap. The SPARC64 VI appears to ship in 2H06 and the SPARC64 VI+ in early 2008.

power number, considering that Fujitsu has doubled the cores and increased the clock frequency but stayed in the same 90nm process. All that logic results in a 540-million-transistor processor and the higher power.

One architectural enhancement now officially included is that each SPARC64 VI core supports dual threads. At last year's speech by Fujitsu's Mr. Aiichiro Inoue, we found out that the cores supported multithreading, but Solaris support had not yet been ironed out with Sun. Obviously, those issues have been resolved since last year, and the dual-threading support will be Solaris compatible.

The Fujitsu threading model is based on coarse-grained multithreading. Each of the threads is called a strand by Fujitsu, and the company refers to the multithreading scheme as vertical multithreading (VMT). The coarse-grained VMT is similar to that used in Intel's Montecito (Itanium) processor. The threading switching occurs on an L2 cache miss, a hardware timer exception, interrupts, and specific multithreading-control instructions. The smaller pipeline bubbles, such as L1 cache miss or load-use penalty, are supposed to be covered by the out-of-order execution engine. The hardware timer will switch threads after the active thread completes a preprogrammed number of cycles and is not reported to software as a processor exception.

The threading hardware overhead is only about 2% of the core gate count. Much of that gate count exists in the duplicated registers needed to support the two-thread (strand) states. The duplicated registers include the general-purpose registers (GPR), the floating-point registers (FPR), the program counter, and the control (state) registers. The number of GPR registers (156) is quite large, making it difficult to maintain a one-cycle access time. To solve the problem, the designers keep a smaller, active copy of the registers, called the current window register (CWR), that has only a one-cycle access time. (See Figure 2.) Because the VMT switches on major events only, the designers believed they could take some extra cycles to copy the registers from the GPRs to the CWRs. The path from the GPR to the CWR files

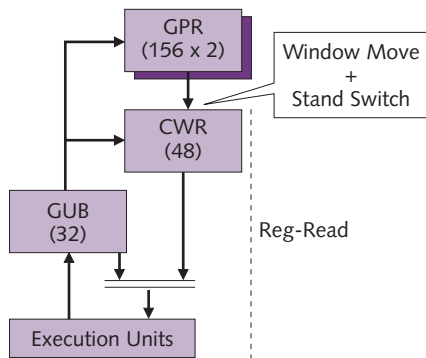


Figure 2. The SPARC64 VI processor has extra sets of registers that are used by the current register window and are backed by the set of two GPR register blocks. The GUB is the rename register file.

is wide and fast, to make the exchange quick when a register window move or strand switch occurs. The general-register update buffer (GUB) provides the renaming registers for the execution units. The execution units can then access operands from either the rename registers (GUB) or the active window register (CWR). The GPR file holds the complete architectural state of both threads.

Performance modeling performed by Fujitsu has shown that the threads do provide additional performance scaling when the number of software threads exceeds the number of cores. (See Figure 3.) Threading cores is a design methodology that appears to have support from both SPARC partners. Sun's highly threaded Niagara processor is expected to ship within a quarter or two at the most.

RAS by Any Other Name

Most of the SPARC die area, including the L2 cache, is covered by one-bit-error-correctable logic. A much smaller area is covered only by one-bit-error-detectable logic, and there is some area where bit errors will not cause an error condition (such as in branch-prediction logic). This is part of the extensive mainframe-class reliability features Fujitsu builds into its SPARC processors. The cache also supports a soft failure mode that allows cache dynamic degradation as cache lines become faulty.

SPARC Doubles Down Again in 65nm

New at FPF05, Fujitsu revealed that its next processor after the SPARC64 VI will increase the number of cores on die to four. All those cores will also be dual threaded. Fujitsu's 65nm process shrink (from 90nm) allows the company to fit four cores and an unknown amount of shared L2 cache into a die size of roughly 21.8mm × 21.3mm. The new processor will

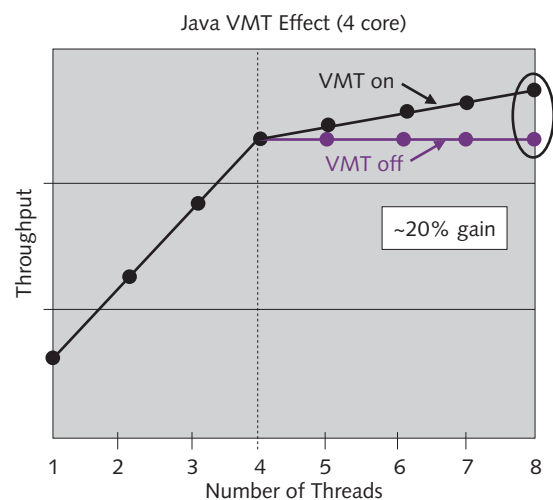


Figure 3. Introducing threads allows the processor to continue to scale and can lead to a gain of up to 20%. This chart shows four threads as the point where scaling levels off, but while the SPARC64 VI has only two cores, the model is for a dual-CPU system.

continue to use the same Jupiter bus as the SPARC64 VI, which Fujitsu believes has enough bandwidth. The use of the same bus is the reason Fujitsu is presently calling the quad-core processor the SPARC64 VI+ instead of bumping the product name to SPARC64 VII. The quad-core processor will not back off core-processor clock frequency, despite the increase in integration, and has a design goal of more than 2.7GHz. During the question and answer part of his presentation, Mr. Maruyama couldn't give us the exact power target, but the rough goal is to be similar to the SPARC64 VI (120W).

These Fujitsu processors, starting shipments in 2006, will become part of the processor lineup that Fujitsu will share with Sun as part of the Advanced Product Line (APL) announced in 2004. (See *MPR 8/2/04-02*, "SPARC's New Roadmap.") The Fujitsu processors should give both companies positive performance improvements in 2006 to be competitive with IBM's Power server processors and Intel's (recently delayed) Montecito Itanium processor.

Sun Makes Its Own Appearance

Prior to FPF05, Sun Microsystems had announced the beginning of UltraSPARC IV+ shipments. The US IV+ is Sun's second generation of dual-core UltraSPARC processors, described at last year's Fall Processor Forum. (See *MPR 10/25/04-02*, "SPARC Turns 90nm.") At that time, Sun's stated goal was to ship the US IV+ at 1.8GHz; Sun's recent announcement was at a somewhat slower 1.5GHz. Of course,

this is not the first time Sun has missed its frequency targets: the UltraSPARC III took a long time to reach 900MHz in late 2000/early 2001. Looking back at Sun's 2000 roadmap provides some amusing examples of Sun's disconnection with reality back then—the company expected to ship a 1.8GHz US IV in late 2002, and the UltraSPARC V (since canceled) would hit 2.1GHz in late 2003.

The US IV+ is reasonably close to the schedule laid out last year of shipping in mid-2005 (it actually shipped in October), and it missed the frequency goal by 300MHz, or 17%. It's a big improvement over Sun's ability to predict processor roadmaps back in 2000. The next big-announcement UltraSPARC for Sun should be the production shipments of its Niagara-based systems before the end of the year.

The UltraSPARC IV and IV+ are not part of the APL sharing, and it is expected that Sun will begin shipping Fujitsu-SPARC64-based servers in late 2006, but Sun will continue to enhance the UltraSPARC IV+ until then. It will be interesting to see how Sun integrates Fujitsu's different product names and Roman-numeral generation codes with Sun's own system (and how many times people will get the IV+ and VI+ confused). Although some competitors like to count the SPARC architecture as headed for the scrap-heap of obsolete Unix/RISC processor architectures, Sun and Fujitsu appear to be stubbornly fending off the junk collector with steady progress and an interesting mix of conservative Japanese design and Silicon Valley risk taking. ♦

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